	L#	Hits	Search Text	DBs
1	L2	34	((detect\$3 determin\$3 diagnos\$3 identif\$6) near10 instruction) near99 ((configuration adj2 (data memory))) and cpu	USPAT; US-PGPUB
2	L1	34	((detect\$3 determin\$3 diagnos\$3 identif\$6) near10 instruction) near99 ((configuration adj2 (data memory))) and cpu	USPAT; US-PGPUB

to the 20 right most bits thereof. bits of the D bus 23 and the right most half (R) referring tively, the left hand side (L) referring to the left most 20 To raisign band selected the selected register of and the D-GRS (L) actions are utilized in loading the above with respect to Table 4 and that the $D\rightarrow GRS(R)$ DI designations refer to the static variables discussed staticizer register 56. It should be noted that the D0 and STAT MEM latch provides the STAT signal for the circuits 41 called STAT MEM. The output of the The STATICIZE action sets a latch in the control the bits provided by bits 11 and 12 of the memory 106.

LYBLE DRIVEN DECISION LOGIC

above where the binary states of the decision points micro control fields illustrated in FIG. 4 were set forth 9. The relationships between the decision points and the ner to be described below with respect to FIGS. 8 and logic 40 (FIGS. 2 and 5) provides 12 decision points vide for conditional control of the computer. Decision 10 requires a plurality of decisions to be made to pro-As discussed above with respect to FIG. 4, the CPU

the class base, the instruction and the interrupt modified to perform a vector jump with respect to tion selected by 1DS where address NAT may be address NAT or NAF in accordance with a func-DPO-controls the real branching by selecting either

tions that provide DPI and DP2 are selected by 4-way conditional vector branch. The logic funccant bits of address NAT respectively to effect a DPI and DP2-are or'ed with the two least signifivectors under control of the XF-field.

by the PDS fields respectively. These decision PI-P4 in accordance with logic functions selected function control fields for the respective processors DP3-DP6-select between the LPFT and LPFF fields VDS0 and VDS1 respectively.

ally place the accumulator contents of the local OUT, WLM, WLMA and SCS field to conditionsion points are utilized in conjunction with the lected by the respective DDS fields. These deci-P3 and P4 in accordance with logic functions secontrol for the respective local processors PI, P2, DP7-DP10-provide deferred action conditional IO in a manner to be described. points control the phantom branching of the CPU

DADS field. cordance with a logic function selected by the the deferred action control table of FIG. 7 in acing between the DACT and DACF addresses into DP11—controls the global deferred action by selectabove with respect to Table 4. static control variables SCI-SC7 as discussed into the local memories 24, 25, 26 and 28 and set the

processors, P1, P2 and P3 onto the D bus 23, write

micro cycle at about to the 100 nanosecond cycle cles. The dynamic variables are computed during a of a micro cycle and may exist over several micro cywhich variables are delineated in Table 4 above. The selectively applied as the inputs to the logic functions static variables and 16 dynamic variables which are the selected logic function. The CPU 10 utilizes 24 Thus, the decisions delineated above are effected by the

selectively provide, in accordance with decision point 10 the general register stack 32 from the D bus 23 respec-As previously discussed, the DACT and DACF ate sign digits from the accumulator. a conventional manner by connections to the appropricither the 18-bit or 36-bit value computed is provided in 5 of the local processors. An indication of the sign of hereinbelow with respect to the configuration control leads to carry look ahead circuitry will be described the generate (G), propagate (P), carry in and carry out

are set in the words read from the memory. deferred actions will occur simultaneously if several bits each combination of deferred actions desired. Several 40 micro instruction. The table 106 includes a word for specify the particular deferred action choices for a Thus, the two control store fields DACT and DACF tails of the control connections will be later described. control the deferred action associated therewith. De- 35 ponents designated by the particular action listed to other bits of the memory 106 are connected to the comtake place, otherwise it will not. In a similar manner, the bit 0 of that word is set to 1, the P-IAR transfer will DACT or DACF selectively under control of DP 11; if 30 addressed in the memory 106 at cither the address strobe input of the register 12. Thus, when a word is connecting the bit 0 output from the memory 106 to the counter 31 to the instruction address register 12 by controls the transfer of the contents of the program 25 determine the selection. Briefly, (referring to FIG. 9) For example, bit 0 which controls the action P→IAR nated actions in accordance with the states of the bits. appropriate control circuitry for effecting the desigontputs from the memory 106 are connected to the each where each bit controls a particular action. The bit 20 DP0-DP11 for effecting the required control in a manexample, the memory 106 includes 28 words of 22 bits master bitted list of the actions to be performed. For with DACT and DACF, the bits thereof providing a storing a plurality of words addressed in accordance ferred action control table 106 comprises a memory for 15 ferred action control table 106 is illustrated. The deglobal deferred actions. Referring now to FIG. 7, decontrol circuits 41 for controlling the performance of II, addresses into a deferred action control table in the itelds of the micro control word in the control store 36

The details for the selective control of the deferred 55 other is loaded into that stage under control of DP 11. BRG register 66 and the bit from one memory or the ories are connected to the least significant stage of the BRG BIT 0 bits from both the DACT and DACF memcontrolled in accordance with DP 11. For example, the 50 bits from the memory are gated at the device to be other addressed by DACF where the corresponding identical memories, one addressed by DACT and the DP 11. This selection is implemented by utilizing two the DACF field is utilized is controlled by the state of 45 106 addressed by the DACT field or that addressed by The choice as to whether the word in the memory

actions control the loading of the BRG register 66 with 13. The LOAD BRG, BRG BIT 0 and BRG BIT 1 the address in the IAR register 12 into the MIR register action causes fetching of the next macro instruction at 65 static variables have values which exist before the start operand address register (OAR) 14. The FETCH VI ister 15 into the main memory at the address in the action controls storing the operand in the MDRW regthe instruction address register 12. The STORE OP D→IAR controls placing the value on the D bus 23 into 60 binary states of the decision points in accordance with cussed hereinabove with respect to FIG. 5. For example tions to be performed refer to register and latches dis-Most of the mnemonics specifying the deferred acactions will be described hereinbelow.

	Docum ent ID	σ	Title	Current
1	US 20040 02512 1 A1		Method of and apparatus for information processing	716/3
2	US 20040 00322 3 A1	Ø	Apparatus and method to decrease boot time and hibernate awaken time of a computer system	713/1
3	US 20030 20479 1 A1	×	Rules-based configuration problem detection	714/48
4	US 20030 05612 8 A1,	⊠	Apparatus and method for a selectable Ron driver impedance	713/300
5	US 20030 03687 4 Al	Ø	Network-based system for configuring a measurement system using configuration information generated based on a user specification	702/123
6	US 20030 00510 4 A1	⊠	Server configuration tool	709/223
7	US 20020 15706 6 A1	☒	Reconfigurable processor devices	716/1
8	US 20020 13369 0 A1	⊠	Semiconductor integrated circuit	712/34
9	US 20020 01667 4 A1	⊠	Golf course yardage and information system having improved zone information and display characteristics	701/215
10	US 20020 01194 9 A1	Ø	Golf course yardage and information system with zone detection	342/357 .06
11	US 20020 01054 4 A1	⊠	Display monitor for golf cart yardage and information system	701/213
12	US 67287 23 B1	☒	Method and system for verifying configuration transactions managed by a centralized database	707/102
13	US 65976 .66 B1.	\B	Method, editor, computer, control module, and storage means for editing configuration data for telecommunications systems	370/254
14	US 65533 95 B2		Reconfigurable processor devices	708/232
15	US 65256 90 B2	☒	Golf course yardage and information system with zone detection	342/357 .13
16	US 64702 42 B1	☒	Display monitor for golf cart yardage and information system	701/1
17	US 64218 17 B1	☒	System and method of computation in a programmable logic device using virtual instructions	716/16
18	US 63538 41 B1	☒	Reconfigurable processor devices	708/232
19	US 63517 97 B1	☒	Translation look-aside buffer for storing region configuration bits and method of operation	711/207

which are utilized for storing masks used in the local addresses thirty-six locations in the local memory 24 provided from the shift/mask address PROM 70 which CPU 10 operates with a 100 nanosecond micro cycle, 10 deferred action. The third input to the multiplexer 80 is memory 24 may be addressed in accordance with a Thus, in a manner to be described hereinafter, the local deferred action control table in the control circuits 41. least significant bits of the D bus 23 under control of the address register (LMAR) 81 which is loaded from the 6 the multiplexer 80 is provided from a local memory rectly under micro program control. A second input to whereby the local memory 24 may be addressed dilocal control field associated with the processor PI

as indicated above with respect to Tables 5 and 12. may be selectively provided from the local memory 24 PROM 70 so that 36 masks as well as their complements memory 24 under control of the shift/mask address 82 is primarily utilized in mask extraction from the local selective complementation control of the complementer B port to the local processor 17 is so provided. The processor 17 is not provided with an internal latch. The register 43 are required since the A port of the local will be later discussed. The latches provided by the A to Table 4. The detailed control of the complementer 82 in the control circuits 41 as indicated above with respect configuration 76 to address the GRS 32 for reading. 25 the field SE from the associated static variable flip-flop 36, the field MC from the instruction status table 38 and control field LMAS is provided from the control store LMAS, MC and SE thereto. It is appreciated that the ory 24 to the A register 83 in either an uncomplemented or complemented form in accordance with inputs will transmit the addressed word from the local mem-A port of the local processor 17. The complementer 82 register 83 which, in turn, provides its 40-bit input to the applied through a complementary \$2 to an A latch The addressed words from the local memory 24 are processor computations.

ment for the CPU 10 to be later described. processor I7 in accordance with the control arrangethat called for by LPFF will be performed by the local of DP3, either the function called for by the LPFT or the decision logic 40. Thus, in accordance with the state input to the multiplexer 84 from decision point 3 from The addressing for the GRS was generally discussed 50 these function control fields is provided by the selection associated with the local processor PL. The selection of LPFF fields of the portion of the micro control word provided from the control store 36 by the LPFT and function latch 85. The 2 inputs to the multiplexer 84 are 5-7, 9-15 are provided from a 2 input multiplexer 84 via a approach. Fourteen of the 16 function bits, namely 50-3, selecting the functions by utilizing a semi-master-bitted approximately 67 functions, the 16-bit function code detail, the local processor 17 has a useful repertoire of provide this address information to RAR3 which is 40 bits 50-515. In a manner to be later described in greater trol for the local processor 17 is provided by 16 function The input, output, arithmetic and logic function con-

local processor function controlled by the S4 function with respect to Table 8. For reasons to be clarified, the specific output control effected was delineated above 65 decision point 7 signal from the decision logic 40. The plexer 86, selection therebetween being effected by the sor are applied respectively to the 2 inputs to the multithe micro control word associated with the PI proceslatch 87. The 2 bits of the OUT field of the portion of port. The S₈ function bit is provided from an accumulathe output of the local processor accumulator to the D The S₈ function bit of the local processor 17 controls

> vide the timing for the GRS writing and reading operachip enable inputs of the multiplexers 77 and 78 to prowill be later described, applies control signals to the 5 sive to timing signals to and tso, which timing signals tively. Additionally, a write enable flip-flop 79 responselection inputs to the multiplexer 77 and 78 respec-GWA fields from the control store 36 are applied as the

In a manner to be further described hereinbelow, the

above with respect to Tables 3 and 9 from which it is described hereinbelow. De bit can merely be concatenated in a manner to be 1108. Because of the boundaries chosen by the 1108, the tive state in a manner identical to that utilized in the whether the x register is in the user state or in the execu- 45 field concatenated with the D6 bit. D6 determines directly from the macro instruction register 13 by the x wide D bus 23. The fourth address source is provided taken from the right 7 of the left 20 bits of the 40-bit cessors 17, 18 and 19 may provide the computations to dressing, is the 'hidden' memory. Any of the local promacro instruction which, in accordance with 1108 adcontains the GRS address provided by the u field of the cant bits of the D4 bus 30. The register RAR3 usually 35 receives this address information from the 7 least signifiof A_0+1 for the 1108 double precision instructions and RAR2 register is usually utilized to contain the address from the 7 least significant bits from the D4 bus 30. The processor 27. The RARI register receives this address 30 ning of the macro instruction emulation by the local which value is generally computed toward the beginister pointed at by the a field of the macro instruction, RARI usually contains the absolute address of the regby the GRA field and transmitted through the OR gate micro cycle one of the four input addresses is selected GRS 32 for writing. During the second half of the is transmitted through the OR gate 76 to address the GWA field during the first half of the micro cycle and 20 words, one of the four input addresses is selected by the GRA and GWA fields from the micro instruction is enabled for reading. Thus, in accordance with the ing the second half of the micro cycle the multiplexer 77 cycle the multiplexer 78 is enabled for writing and dur- 15 tso it is reset. Thus, during the first half of the micro ciated that at to the write enable flip-flop 79 is set and at the strobes being designated as to-190. Thus, it is appretiming strobes being provided every ten nanoseconds,

the control store 36. the GRA and GWA fields in the micro instructions in vided to the register address registers 33 as directed by 55 field from the IST memory 38, the results being proformed by the local processor 27 in response to the GB appreciated that the base address computations are per-

multiplexer 80 is provided by the LMA field from the above with respect to Table 5. One of the inputs to the sor P1 provided from the control store 36 as discussed from the local control field associated with the proces-80 where the inputs are selected by the LMAS field memory 24 is addressed by a 6-bit, 3 input multiplexer 25 and 26 are 64 words long by 40 bits wide. The local therewith respectively. Each of the local memories 24, which have local memories 24, 25 and 26 associated 60 tor output control multiplexer 86 via an Sg function processors 17, 18 and 19 designated as P1, P2 and P3 As previously discussed, the CPU 10 includes local

	Docum			Current
	ent	ט	Title	OR
20	US 62893 96 B1	Ø	Dynamic programmable mode switching device driver architecture	719/323
21	US 62369 40 B1	×	Display monitor for golf cart yardage and information system	701/300
22	US 62363 60 B1	⊠	Golf course yardage and information system	342/357 .13
23	US 61725 21 B1	⊠	Programmable logic IC having memories for previously storing a plurality of configuration data and a method of reconfigurating same	326/40
24	US 60650 67 A	☒	System, method and program for controlling access to an input/output device possible resource settings data in an advanced configuration and power interface operating system	710/8
25	US 60471 15 A		Method for configuring FPGA memory planes for virtual hardware computation	716/16
26	US 58783 69 A	⊠	Golf course yardage and information system	701/215
27	US 58601 33 A	⊠	Method for altering memory configuration and sizing memory modules while maintaining software code stream coherence	711/171
28	US 57520 35 A	⊠	Method for compiling and executing programs for reprogrammable instruction set accelerator	717/153
29	US 57489 79 A	☒	Reprogrammable instruction set accelerator using a plurality of programmable execution units and an instruction page table	712/37
30	US 56894 31 A	☒	Golf course yardage and information system	701/213
31	US 51795 30 A		Architecture for integrated concurrent vector signal processor	708/520
32	US 49891 37 A	Ø	Computer memory system	711/203
33	US 49673 40 A	⊠	Adaptive processing system having an array of individually configurable processing components	712/19
34	US 47759 32 A	⊠	Computer memory system with parallel garbage collection independent from an associated user processor	707/206

ahifter are 0. indication when all of the bits transmitted through the dynamic variable in the CPU 10 which provides an 10 and also provides a ZERO detect output utilized as a bi-directional port for the most aignificant bit (MSB) tional port for the least significant bit (LSB) as well as a and the ALU 101. The shifter 104 includes a bi-direcinput to the A bus multiplexer 100, the B bus latch 103 The output of the accumulator 105 is also applied as an vides the value to the output D port of the processor. tor 105 (designated as a) whose output, in turn, proshifter 104 whose output is applied to a micro accumula-The output from the ALU 101 is applied to a 1-bit

inputs to the decision logic 40 as variables into decision the respective processors 17, 18, 19 and 27 provide The overflow outputs from the most significant chips of 60 processor as delineated above with respect to Table 4. provide the ZERO detect dynamic variable for the chips comprising a processor are ANDed together to higher order chip. The ZERO detect output from the output of a chip connected to the LSB of the next 104 for all of the chips in a processor are serially conthe chips comprising a processor. The shifter circuits tion control bits 50-515 are applied in parallel to all of each of the local processors 17, 18, 19 and 27, the func-30 memory 28, B4, bus 29 and D4 bus 30, respectively. For ports being connected in parallel to the 20-bit wide such chips with the resulting 20-bit wide A, B, and D respectively. The local processor 27 is comprised of 5 the 40-bit wide A bus register 83, B bus 22 and D bus 23 45 40-bit wide A, B, and D ports connected in parallel to as illustrated in FIG. 6 are utilized with the resulting local processors 17, 18 and 19, 10 4-bit wide chips such the circuits in parallel. Specifically, in implementing the the 20-bits required by the processor 27 by connecting 40 40-bits required by the processors 17, 18 and 19 and to parallel to the data flow. The chip is expanded to the Each of the chips utilized is 4-bit wide and is sliced mented in said Motorola specification referenced above. as the details of its structure and operation are docu-35 capability. The complete repertoire for the chip as well chip, the external A register 83 is utilized to provide this Since there is no internal latch for the A port of the latched in the accumulator 105 at the end of a cycle. micro cycle and the result of the last operation is 30 is latched in the B bus latch 103 at the beginning of each with respect to FIGS, 2 and 5. Data from the B bus 22 external high speed shifter 35 is utilized as described shift 104 is constrained to a 1-bit shift per cycle, the micro cycle utilizing the mask network 102. Since the 25 function followed by an arithmetic function in the same Additionally, the chip can perform a Boolean logic repertoire is AND, OR, EXCLUSIVE OR and NOT. subtract, complement, shift I bit and the basic logic the D bus 23. The basic arithmetic repertoire is add, 20 the function bit 58 permitting the wired OR output to viously described, the D port output can be disabled by lected by the semi-master-bitted inputs So-S15. As pre-67 functions. As discussed above, the functions are sefunctions, the chip having a repertoire of approximately 15 functions, binary arithmetic and a set of data routing The chip illustrated in FIG. 6 provides Boolean logic

processors in the 2×20 bit mode. The connections of utilized interconnected in a 36-bit mode or as 2, 20-bit ing each of the local processors 17, 18 and 19 may be As previously described, the 10 4-bit chips compris-

logic circuits to be described hereinbelow.

convenience be designated as a block 88. to the S4 input. The components 80, 82-87 may for function is disabled by applying a permanent "1" signal bit is not utilized in the operation of the CPU 10 and the

to the block 88. 88" for reasons similar to those discussed with respect address PROM 70 provide inputs to the blocks 88' and local memory address register 81 and the shift/mask fields from the control store 36 are applied thereto. The exception that appropriately associated local control blocks 88' and 88" are identical to the block 88 with the processor 19 and the local memory 26 is a lock 88". The memory 25 is a block 88' and associated with the local Associated with the local processor 18 and local

processor 17. for the reasons discussed above with respect to the processor 27 is permanently disabled in the manner and which it exclusively provides inputs. The Seinput to the since the processor II utilizes the private D4 bus 30 to 89. The S₈ input is permanently enabled by a 1 input from one of the function bit outputs of the multiplexer processor 27 is treated as a function bit and is provided the decision logic 40. The carry in (CIN) input to the LPFT and LPFF is effected by decision point 6 from above with respect to FIG. 4. The selection between word associated with the P4 processor as discussed LPFT and LPFF from the portion of the micro control control store 36 by the local processor function fields The 2 inputs to the multiplexer 89 are provided from the a function select multiplexer 89 via a function latch 90. function bits 50-3, 5-7, 9-15 are provided in parallel from scribed above with respect to the processor 17. The 16 function bits So-S15 in a manner similar to that deto the blocks 63 and 64. The local processor 27 utilizes memory 28 has previously been discussed with respect processor 17, 18 and 19. The addressing of the local ory 28 is configured somewhat differently from the The local processor 27 with its associated local mem-

bus respectively. sponds to the Motorola terminology A bus, O bus and I lized herein, namely, A bus, B bus and D bus, correucts, Inc. it should be noted that the terminology uti-1976, available from Motorola Semiconductor Prod-FORMANCE MECL LSI PROCESSOR FAMILY" found in the publication entitled "M10800-HIGH PER-The detailed specifications for this ALU slice may be 4-bit slice ALU was selected for the implementation. processor variety. Particularly, the Motorola 10,800 preferably constructed from LSI chips of the micro Each of the local processors 17, 18, 19 and 27 are

ate (G), carry propagate (P), as well as overflow and CRITY in signal. The ALU 101 also provides carry genertion select bits 50-515 as discussed above as well as a 65 the ALU block 101. The ALU 101 receives the 16 funcwell as the output from the latch 103 provide inputs to micro cycle. The output of the mask network 102 as from the B bus 22 (FIG. 5) at the beginning of each provided from a B bus latch 103 utilized to latch values network 102. Another input to the mask network 102 is applied to the ALU 101 of the chip as well as to a mask applied as an input to a multiplexer 100 whose output is input from the A register 83 (FIG. 5) to the A port is nents and paths that are utilized in the CPU 10. The 35 nected with respect to each other with the MSB shifter sors 17, 18, 19, and 27 is utilized depicting the compoof the ALU slice utilized to implement the local proces-Referring now to FIG. 6, a schematic block diagram

carry out signals.